CLAIM SET AS AMENDED

IN THE CLAIMS

17. (Currently amended) A scaleable integrated data processing device, provided on a carrier substrate ~~(S)~~, comprising a processing unit having one or more processors, and a storage unit having one or more memories,

wherein the data processing device comprises mutually adjacent, substantially parallel stacked layers ~~(P,M,MP)~~ and the processing unit and the storage unit are provided in one or more of the substantially parallel stacked layers,

wherein each of the substantially parallel stacked layers comprises one or more processors and/or one or more memories, and electrical conducting structures which form internal electrical connections in the layer,

wherein each substantially parallel stacked layer is formed of a plurality of sublayers, having delimited portions which form dielectric, semiconducting or electrical conducting areas in the sublayer and the sublayer, in addition to at least one dielectric portion, having one or more semiconducting and/or electrical conducting portions,

wherein delimited portions with a given electrical property in each sublayer are provided in a registering relationship to one or more corresponding portions in at least one of the adjacent neighbor sublayers to form integrated circuit elements which extend vertically through one or more sublayers,

wherein the electrical conducting structures are formed by the electrical conducting portions in the sublayer and respectively extend horizontally in order to create horizontal electrical conducting structures or are provided in registering connection with corresponding electrical conducting portions in one or more adjacent sublayers, such that the electrical conducting structures integrated in the sublayers form three-dimensional electrical interconnecting networks in the layers and interconnect the circuit elements therein mutually in three dimensions, and

wherein additional electrical conducting structures in the data-processing device interconnect the layers mutually and/or the layers with the substrate and in order to create a connection to the exterior of the data processing device.

18. (Currently amended) A scaleable integrated data processing device according to claim 17, wherein the sublayers in one or more of the substantially parallel stacked layers are realized in a technology which on a first level of a functional hierarchy configures functionally one or more of the layers as a combined processor and memory layer ~~(MP)~~, or one or more the layers substantially as processor layers ~~(P)~~ or one or more the layers substantially as memory layers ~~(M)~~.

19. (Currently amended) A scaleable integrated data processing device according to claim 18, wherein the processing unit in a layer ~~(P, MP)~~ is

configured functionally on a second level of the functional hierarchy as one or more processors ~~(5)~~ or parts of one or more processors ~~(5)~~, at least one processor constituting a central processing unit or microprocessor ~~(5)~~ in the data processing device, and possible further processors optionally being configured as control and/or communication processors respectively.

20. (Currently amended) A scaleable integrated data processing device according to claim 19, wherein the central processing unit ~~(5)~~ is configured functionally on a third level of the functional hierarchy as a parallel processor with several execution units working in parallel provided in one and the same layer ~~(P, MP)~~ or in two or more layers ~~(P, MP)~~ or in sublayers thereof to provide an optimal interconnection topology.

21. (Currently amended) A scaleable integrated data processing device according to claim 19, wherein more than one central processing unit is provided, wherein each central processing unit ~~(5)~~ is mutually interconnected and adapted for working in parallel and provided in one and the same layer ~~(P, MP)~~ or in two or more layers ~~(P, MP)~~ to provide an optimal interconnection topology.

22. (Currently amended) A scaleable integrated data processing device according to claim 19, wherein the storage unit in a layer ~~(M,MP)~~ is configured functionally on the second level of the functional hierarchy as one or more

memories or parts of one or more memories, at least one memory constituting a RAM and being connected with at least one control processing unit or microprocessor, and possible further memories optionally being configured as high-speed memories, ROMs, WORM, ERASABLE and REWRITEABLE respectively.

23. (Currently amended) A scaleable integrated data processing device according to claim 22, wherein two or more RAMs ~~(6)~~ are connected to a central processing unit ~~(5)~~ and respectively assigned to two or more subunits in the central processing unit ~~(5)~~, RAMs ~~(6)~~ and the subunits being distributed in selected combinations in one or more layers ~~(P, M, MP)~~ to provide an optimal interconnection topology.

24. (Currently amended) A scaleable integrated data processing device according to claim 22, wherein two or more central processing units ~~(5)~~ are provided which are connected with one or more common RAM or RAMs ~~(6)~~, and each central processing unit is provided in mutually adjacent layers ~~(P, MP)~~, or distributed in selected combinations between two or more layers ~~(P, MP)~~, and that the common RAM or RAMs are provided in selected combinations in one or more of the layers ~~(P, MP)~~ and/or in one or more memory layers ~~(M)~~ adjacent to the latter or interfoliated there between to provide an optimal interconnection topology.

25. (Previously amended) A scaleable integrated data processing device according to claim 22, wherein at least a part of the storage unit constitutes a mass memory, the mass memory optionally being configured as RAM, ROM, WORM, ERASABLE or REWRITEABLE or combinations thereof.

26. (Currently amended) A scaleable integrated data processing device according to claim 18, wherein the data processing unit comprises several processor layers ~~(P)~~ and several memory layers ~~(M)~~, and the memory layers ~~(M)~~, in order to reduce the signal paths there between and the processor layers ~~(P)~~, are interfoliated between the latter.

27. (Currently amended) A scaleable integrated data processing device according to claim 17, wherein further electrical structures are provided as electrical edge connections on or over at least one side edge of one or more layers ~~(P,M,MP)~~ in order to contact electrical conducting structures in other layers and/or provide electrical connection between layers and substrate.

28. (Currently amended) A scaleable integrated data processing device according to claim 17, wherein the further electrical conducting structures are provided as vertical conducting structures in one or more layers ~~(P, M, MP)~~ and form electrical connections in the cross-direction of the layers and perpendicular to their planes in order to contact electrical conducting structures in other layers and/or to provide electrical connection between the layers and substrate.

29. (Currently amended) A scaleable integrated data processing device according to claim 17, wherein one or more layers ~~(P, M, MP)~~ are formed of an organic thin-film material, the organic thin-film material or materials selected from the group consisting of monomeric, oligomeric and polymeric organic materials and metal-organic complexes, and combinations thereof.

30. (Currently amended) A scaleable integrated data processing device according to claim 29, wherein all layers ~~(P, M, MP)~~ are formed of organic thin-film material.

31. (Currently amended) A scaleable integrated data processing device according to claim 17, wherein one or more layers ~~(P, M, MP)~~ are formed of inorganic thin-film material, the inorganic thin-film material or materials being selected from the group consisting of crystalline, polycrystalline and amorphous thin-film materials, and combinations thereof.

32. (Currently amended) A scaleable integrated data processing device according to claim 17, wherein two or more layers ~~(P, M, MP)~~ are formed of both organic and inorganic thin-film materials or combinations thereof, the organic thin-film material or materials being selected from the group consisting of monomeric, oligomeric and polymeric organic materials and metal-organic complexes, and combinations thereof, and the inorganic thin-film material or

materials being selected from the group consisting of crystalline, polycrystalline and amorphous thin-film materials, and combinations thereof.

33. (New) A data processing device, comprising:

a carrier substrate; and

a plurality of main layers formed above the carrier-substrate, wherein each main layer is one of a processor layer, a memory layer, or a combination layer, and wherein at least one main layer includes logic devices formed from organic materials.

34. (New) The data processing device of claim 33, wherein the at least one main layer comprises a plurality of vertically stacked sublayers, wherein:

at least one sublayer includes at least one horizontally conducting structure for electrically connecting logic devices; and

at least one sublayer includes at least one vertically conducting portion for electrically connecting logic devices.

35. (New) The data processing device of claim 34, wherein at least one vertically conducting structure is formed from aligned corresponding vertically conducting portions of at least two adjacent sublayers.

36. (New) The data processing device of claim 34, wherein the logic devices of the at least one main layer are formed to extend vertically through at least one sublayer.

37. (New) The data processing device of claim 34, wherein portions of an organic material layer of the at least one sublayer are configured to have varying mode and degree of electrical conductivity.

38. (New) The data processing device of claim 37, wherein the organic material layer at least one of polymer molecules, aromatic molecules, polyaniline films, and polythienylene vinylene films.

39. (New) The data processing device of claim 37, wherein the electrical conductivity of the organic material layer is accomplished through application of at least one of electrical fields, voltages, currents, photon radiation, and particle radiation.

40. (New) The data processing device of claim 33, wherein a first main layer formed directly above the carrier substrate is formed from a plurality of sublayers, wherein at least one sublayer of the main layer is based on inorganic technology.

41. (New) the data processing device of claim 40, wherein the at least one sublayer is based on silicon or on thin film technology.

42. (New) The data processing device of claim 33, wherein a memory portion of at least one memory layer or at least one combination layer comprises:

a plurality of substantially parallel overlying electrodes;

a plurality of substantially parallel underlying electrodes, wherein the overlying and underlying electrodes intersect to form a matrix; and

a plurality of logic cells formed at the intersections of the matrix.

43. (New) The data processing device of claim 42, wherein the underlying electrode is made from a material with a lower work function relative to the overlying electrode, and wherein at least one logic cell comprises:

a first polymer in contact with the underlying electrode;

a second polymer in contact with the overlying electrode; and

a third polymer formed between the first and second polymers, such that the first, second, and third polymers form a rectifying diode.

44. (New) The data processing device of claim 43, wherein:

the first and second polymers are formed from polythiophene; and

the third polymer is formed from water-soluable polythiophene.

45. (New) The data processing device of claim 42, wherein at least one logic cell is formed from ferroelectric material.

46. (New) The data processing device of claim 42, wherein at least one logic cell is configured to store more than two levels of code.

47. (New) A method to fabricate a data processing device, comprising:

forming a carrier substrate; and

forming a plurality of main layers above the carrier-substrate, wherein each main layer is one of a processor layer, a memory layer, or a combination layer, and wherein at least one main layer includes logic devices formed from organic materials.

48. (New) The method of claim 47, wherein the step of forming the plurality of main layers comprises forming at least one main layer from a plurality of vertically stacked sublayers, wherein forming the plurality of vertically stacked sublayers includes:

forming at least one horizontally conducting structure for electrically connecting logic devices in at least one sublayer of the vertically stacked sublayers; and

forming at least one vertically conducting portion for electrically connecting logic devices in the at least one sublayer.

49. (New) The method of claim 48, further comprising forming at least one vertically conducting structure by aligning corresponding vertically conducting portions of at least two adjacent sublayers.

50. (New) The method of claim 48, further comprising forming the logic devices of the at least one main layer to extend vertically through at least one sublayer.

51. (New) The method of claim 48, further comprising configuring portions of an organic material layer of the at least one sublayer to have varying mode and degree of electrical conductivity.

52. (New) The method of claim 51, wherein the organic material layer at least one of polymer molecules, aromatic molecules, polyaniline films, and polythienylene vinylene films.

53. (New) The method of claim 51, wherein the step of configuring electrical conductivity of the organic material layer comprises applying at least one of electrical fields, voltages, currents, photon radiation, and particle radiation to the organic material layer.

54. (New) The method of claim 47, wherein a step of forming a first main layer formed directly above the carrier substrate comprises forming a plurality of sublayers, wherein at least one sublayer of the main layer is based on inorganic technology.

55. (New) the method of claim 54, wherein the at least one sublayer is based on silicon or on thin film technology.

56. (New) The method of claim 47, wherein a step of forming a memory portion of at least one memory layer or at least one combination layer comprises:

forming a plurality of substantially parallel overlying electrodes;

forming a plurality of substantially parallel underlying electrodes, wherein the overlying and underlying electrodes intersect to form a matrix; and

forming a plurality of logic cells formed at the intersections of the matrix.

57. (New) The method of claim 56, further comprising configuring the at least one logic cell to store more than two levels of code.

58. (New) The scaleable integrated data processing device of claim 17, wherein one or more of the plurality of sublayers is formed from organic materials.

AMENDMENTS TO THE DRAWINGS

Please substitute the attached FIG. 1 for that originally filed.